CURRICULUM VITAE

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GENERAL INFO AND EDUCATION

Nationality	Italian
Place and Date of Birth:	Milan 14/01/1957.
Languages:	Italian mother-tongue. Fluent in English and French.
Education background:	Master Degree in Electronic Engineering (M.Eng.) University of Rome "La Sapienza", 1985, graduation thesis: "Interactive layout of sparse diagrams algorithms", advisor Prof. Carlo Batini.
Professional certification:	Qualifying examination, November '85.
Professional registration:	Member of the Professional Engineer List of L'Aquila (n.1641 date:07/12/2001).

SKILLS AND COMPETENCES

I had basically developing a technical career working for the main telecommunication companies (Italtel, AT&T, Nokia-Siemens, Alcatel and currently, the Ericsson) designing complex systems like crossconnects, add-drop multiplexer, dslam, layer 2 switches, etc.. with specific responsibilities in:
- research, design and development teams management,
- project management and technical coordinator activities,
- system requirement analysis and specification,
- system architecture and design.

the main systems characteristics and functionalities are:
- multiprocessor, distributed intelligence, hard real time and embedded software systems,
- protocol stacks for either data and control plane (IP, ATM, SDH, PDH, etc..),
- covering functional areas like fault and performance management, protection switching, etc..,
- system configuration based on MIB interface designed in both SNMP and TMN context.

My research interests and activities are in software engineering areas like:
- requirement engineering,
- model driven design and UML,
- model checking,
- software performance analysis,
- automatic test generation end execution.

At the moment I'm collaborating with the Computer Science Department of L'Aquila University as a contract lecturer of Data Base Labs teaching course.

RELEVANT ACCOMPLISHMENTS

2005 onwards

company: **Intecs S.p.A. (Ex Technolabs S.p.A.)** - S.S. 17, I-67100, L'Aquila
business type: Telecommunication, R&D Labs
my role: System & Software Architect

- (Ericsson - Genoa, Italy) consultant on OMS1600 and OMS1200 cross-connect systems.
- (Ansaldo – Naples, Italy) consultant on network infrastructure design of the train traffic control system of the Torino-Verona section.
- (Alcatel - Milan, Italy) consultant on MPR-E Wireless System Management Interface and to introduce UML in system design lifecycle.
- (Technolabs – L'Aquila, Italy) Architecture team member on:
    - mrDSLAM: mini radio DSLAM,
    - DVB-ASI: video streem over SDH network interface system,
    - CipHop, ODU_IP, WideHop: L2-switch and SDH microwave wireless systems

2004 onwards

company: ***University of L'Aquila*** - Information Engineering, Computer Science and Mathematics Department (DISIM) - *Coppito, I-67100, L'Aquila*
my role: Contract Lecturer

- lecturer on Data Base Labs teaching course of Computer Science Department
- research on Software Engineering area: "model-based software performance analysis", "requirement quality analysis" and "model-checking and test generation"

1997 - 2005

company: **SIEMENS CNX S.p.A.** - S.S. 17, I-67100, L'Aquila
business type: Telecommunication, R&D Labs
my role: System & Software Architect

- (Siemens CNX – L'Aquila, Italy) Architecture team member on Q3 and SNMP management interface definition for the hiT70xx family
- (Siemens AS – Munich, Germany) Architecture team member on specification of the GMPLS architecture over hiT70xx node networks.
- (Siemens AS – Munich, Germany) Architecture team member on specification of the hiT7070 10Gbe interface with Layer 2 switch capability
- r(Siemens CNX – L'Aquila, Italy) Architecture team member on equirement specification and architecture design of hiT7070 and hiT7050, respectively, cross-connect and add/drop multiplexer systems belonging to the hiT70xx family.
- involved in partnership research program with the L'Aquila University cooperating with the Computer Science Department on software engineering field.

1990 – 1997

company: **ITALTEL S.p.A.** - L'Aquila
business type: Telecommunication, R&D Lab
my role: Software area manager

- (AT&T-Bell Labs – Denver, CO USA) Architecture team member on the SDM4 synchronous multiplexer and the DACS VI-2000 cross-connect systems;
- (AT&T-NSI – Huizen, Netherlands) Design and development of the ISM2000 SDH

add-drop multiplexer systems;
- (Italtel – Milan, Italy) Design and development of the OLC2000 POTS access system

1985 - 1990

company: **Selenia S.p.A.** (now Selex ES, Finmeccanica company) - Roma - Radar & System division

business type: Electronics, Air Traffic Control Systems

my role: System Engineer, Software designer and developper

- (C.A.A. - Camberra, Australia) Architecture Team Member for the Australian ATC System project, coordinated by the Australian CAA.
- (C.A.A. - Doha, Qatar) Software design manager for the Qatar ATC system;
- (C.A.A. - Hong Kong) Software Integration Test and Continuity Test of Hong Kong ATC system in Kai Tak international airport;
- (Selenia S.p.A. - Rome, Italy) Software design, development of flight data plane subsystem;
- (Selenia S.p.A. - Rome, Italy) Software design, development and integration of the ATC display subsystem;

MAIN INTERNATIONAL EXPERIENCE

2005	*Paris (France)*	13th IEEE International Requirements Engineering Conference RE2005
2005	*Seattle-WA (USA)*	IEEE International Symposium on Object-Oriented, Real Time Distributed Computing ISORC2005
2004	*Toledo (Spain)*	1st International Workshop on Integration of Testing Methodologies ITM2004
1997/2005	*Monaco c/o Siemens*	Architecture Team member on SURPASS hiT70xx series
1993/94	*Denver-CA (USA) AT&T Bell Labs*	Architecture Team member for STM-4 synchronous multiplexer and DACS-VI 2000 cross-connect systems design.
1991	*Huizen (Olanda) AT&T NSI*	Design of subscriber access subsystem of the STM-1 synchronous multiplexer.
19988/90	*Camberra (Australia) CAA Australia*	Analysis & Design Team member of ATC Australia system.
1988	*Doha (Qatar) international airport*	Software design manager of ATC Quatar system.
1987	*Hong Kong international airport*	ATC HK system in field validation tests.

RESEARCH AND PUBLICATIONS

MOSES - Software Performance Analysis

Coordinated with **Prof. V. Cortellessa** of Computer Science Department of University of L'Aquila

Several methodologies have been proposed in literature to cover the performance analysis of a software system.
The aim of our approach is to provide a methodology that is:

- easy to use by the software designers,
- easy to integrate in the software development lifecycle,
- applicable since the preliminary software modeling phases,
- allowing predicting performance parameters with significant precision.

The core of the methodology consists on integrating the UML model of the application software with a platform model then simulating the resulting performance model to compute and predict the software system performances.
In addition, a library of hardware prototypes, probes, workload generators and other utility modules has been defined to simplify the creation of the platform models and the integration and simulation of the resulting performance model..
This methodology has been adopted by the PRESTO project (Im**P**rovements of Industrial **R**eal Time **E**mbedded **S**ys**T**ems Development pr**O**cess), co-funded by the European Commission under the ARTEMIS Joint Undertaking Programme

publication

- V. Cortellessa, P. Pierini, R. Spalazzese, A. Vianale (2008): "***MOSES: MOdeling Software and platform architEcture in UML2 for Simulation-based performance analysis".*** 4th International Conference on the Quality and Software Architecture QoSA, October 2008, Karlsrhue, Germany.
- V. Cortellessa, P. Pierini, D. Rossi (2007): ***"Integrating software models and platform models for performance analysis".*** IEEE Transaction on Software Engineering, June 2007, Vol.33 n.6
- V. Cortellessa, P. Pierini, D. Rossi (2005): ***"On the adequacy of UML-RT for performance validation of an SDH telecommunication system".***
IEEE International Symposium on Object-Oriented, Real Time Distributed Computing ISORC 2005, May 2005, Seattle, WA (USA).

stages

- R. Spalazzese - Performance validation through integrated software and platform models
- D. Rossi - Performance Analysis in telecommunication software development

thesis

- A. Vianale - performance analysis over UML2 software models (July 2007)
- N. Stivaletta - Integrating a performance model from UML-RT SW and platform models (Jul. 2007)
- D. Rossi - Performance Analysis on UML-RT models of telecommunication system software

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TESTOR - Model checking + testing

Coordinated with **Prof. H. Muccini** of Computer Science Department of University of L'Aquila and the participation of **Prof. P. Pelliccione**.

In the system development lifecycle, a system architecture (SA) is defined on the basis of a given set of system requirement. Then, starting form the architecture, the system is developed. At the end, a set of functional tests must be performed on the implemented system to prove its conformance to the requirements.
The basic idea of this research born from the consideration that the functional tests of an implemented system, that verify its conformance to the given set of requirements, should be supeseded if the SA model has been already checked for requirements conformance. Instead, the implemented system should be checked for its conformance to the system architecture.
This research try to redesign the flow of the development lifecycle taking advantage of the model-

checking (MC) technique to exhaustively and automatically validate a SA model with respect to a given set of requirements.
In addition, the results of the MC validation has been further utilised to automatically obtain the test case specification for conformance checking of the implementation to the SA model.
TeStor is an original automated algorithm able to derive test cases from a validated SA model. It has been implemented as a plugin of the tool **Charmy** (CHecking ARchitectural Model consistencY) based on the SPIN model checker.

publication

- A. Bucchiarone, H. Muccini, P. Pelliccione, P. Pierini (2005): ***"An Architecture-centric Approach for Model-checking based Testing in Industrial Contexts"***
Technical Report, April 2005, L'Aquila, Italy.
- A. Bucchiarone, H. Muccini, P. Pelliccione, P. Pierini (2004): ***"Model-Checking plus Testing: from Software Architecture Analysis to Code Testing"***
1st International Workshop on Integration of Testing Methodologies ITM 2004, October, 2004, Toledo, Spain.
- A. Bucchiarone, H. Muccini, P. Pelliccione, P. Pierini (2004): ***"Software Architecture-driven System Testing through Model-Checking".***
IPAS: 2004E17318 IT, Invention Report, August 2004, L'Aquila, Italy

stages

- E. Di Nisio - applicazione di tecniche di model checking per la verifica di conformita' di un modello architetturale in relazione alle proprieta'

thesis

- C. Filippi - Software Architecture based testing

MDE - Model Driven Engineering

Coordinated with **Prof.sa P. Inverardi** of Computer Science Department of University of L'Aquila.

stages

- A. Bucchiarone - adopting UML methodology and CASE tools for TLC system design.
- L. Berardinelli - A metamodel approach to reverse engineering from SMIv2 to UML2.

thesis

- M. Di Donatantonio - Automatic code generation, an industrial case study.

RE - Requirement Engineering

Coordinated with **Prof.sa S. Gnesi** at ISTI-CNR of Pisa and the participation of **A. Bucchiarone**.

The requirements of the SXA SDH crossconnect system, managed with RequisitePro, has been submitted to the **QuARS** (Quality Analyzer for Requirement Specifications) provided by the ISTI-CNR of Pisa. This case study allowed to experiment the integration of QuARS with requirement management tools. In addition, the analysis demonstrate the high quality of the given requirements with very good lexical and syntactical indicators but a small criticality of the general readability of the SRS document.

publication

- A. Bucchiarone, S. Gnesi and P. Pierini (2005): ***"Quality Analysis of Natural Language Requirements: An Industrial Case Study"***
13th IEEE International Requirements Engineering Conference, August 2005, Paris, France.

PARTICIPATION TO INTERNATIONAL COMMITEES

- 2007-2011: Member of the "Comitato Elettrotecnico Italiano" (CEI) Technical Committee CT57 "Information model related to power system management".
- ICCES'07, ICCES'08: External reviewer of International Conference on Computer Engineering & Systems 2008 and 2009.

PATENTS

- R. Capezzali, P. Ciammaichella, P. Illuminati, P. Pierini (2005): ***"Distributed overhead cross-connection".***
  IPAS: 2005E01150 IT, Patent MI2005A001794, September 2005, Milano, Italy
- A. Bucchiarone, H. Muccini, P. Pelliccione, P. Pierini (2004): ***"Software Architecture-driven System Testing through Model-Checking".***
  IPAS: 2004E17318 IT, Invention Report, August 2004, L'Aquila, Italy.

I authorize the use of personal data in observance of the privacy statements of Italian law (DLgs 196/03).

L'Aquila, July 2015

Yours Sincerily
Pierluigi Pierini